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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/681,068
Filing Date: October 07, 2003
Appellant(s): HILDEBRANT ET AL.

Gregory W. Osterloth
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 22 October 2010 appealing from the Office action mailed 15 March 2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application: Claims 1-17.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the

subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

5,257,268	Agrawal	03-1990

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Agrawal (US 5,257,268).

Regarding claims 1, 8 and 13; Agrawal discloses a machine-executable method comprising executing sequences of instructions on a machine, the executed sequences of instructions causing the machine to perform the actions of, (col. 4:33-35), reading a test file having a plurality of test vectors, (col. 3:65-4:1), where the test unit reads previously supplied initialization vectors; determining a required memory needed to execute the plurality of test vectors, (col. 4:40-60), when the system determined the minimum required number of flip-flop gates (memory); and using the required memory to estimate a cost to execute the test vectors, (col. 4:50-52), one of the computed cost functions being equal to the number of required flip-flops (memory).

Regarding claims 2 and 14; Agrawal discloses wherein the executed sequences of instructions further cause the machine to perform the action of receiving a

billing scheme and wherein using the required memory to estimate a cost includes using the billing scheme to estimate the cost to execute the test vectors,(col. 5:57-61) where the system takes in consideration the budget requirements or "billing scheme".

Regarding claims 3, 10 and 15; Agrawal discloses determining a required memory comprises determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board,(col. 6:50-68), multi-level hardware such as multiple boards circuitry is expressed as multiple levels of gate arrays and the cost is estimated by a total of the gates in each level.

Regarding claims 4, 11 and 16; Agrawal discloses determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin, (col. 1:16-30).

Regarding claims 5 and 12; Agrawal discloses wherein determining a required memory comprises counting the number of test vectors for each of one or more tests in the test file, (col. 4:49-68), wherein selecting the various trail vectors there is memory allocated to each test vector output.

Regarding claim 7; Park discloses wherein the executed sequences of instructions further cause the machine to perform the action of, for each additional test in the test file: for each pin of the tester, determining a third memory requirement for the pin to execute the test vectors for the additional test; and setting the required memory equal to the third memory requirement if the third memory requirement is greater than the required memory, (col. 6:62-68), defining the minimum cost one would has to conclude that it is the largest value of the absolutely required amount.

Regarding claim 9: Agrawal discloses wherein the machine further comprises a user interface to display the cost to a user, (col. 5:30-37), where the system has user

input devices or GUI to interface with the program by setting parameters such as acceptable cost limits.

Claims 6 and 17 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Agrawal (US 5,257,268).

Regarding claims 6 and 17; Agrawal discloses determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file; setting the required memory equal to the first memory requirement; and for each additional pin of the tester, determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement, (col. 6:46-68), wherein the minimum required memory is all summed up depending of the architecture of the CUT (circuit under test), and all the memory required for every pin input and output is totaled. Since all test sequences are done sequentially, it is inherent for the system to generate a signal for every test point input for the duration of the longest sequence or vector. That is if the longest instruction sequence takes 11 clock pulses, then for every input of the CUT there must be 11 sequenced values stepped through with the clock pulses, each value retained in its own memory address.

It should be understood that all limitations of claims 6 and 17 are covered by Agrawal yet in an ambiguous manner and that although inherent in the disclosure it would also surely be obvious to one of ordinary skill in the art to interpret the computing of the test vectors costs for all inputs to mean that each input will analyzed and vectors generated for them, the embodiments as such, infers that all inputs are being tested in that means each and every one input stating with a first input and going down to the last input.

(10) Response to Argument

1. The examiner views the appellant's invention as claimed; execution of instructions; reading a test file; determining a required memory needed to execute a plurality of test vectors and estimating the cost of executing the test vectors. The claim language doesn't specify the method of determination not the method of estimation of cost. Where Agrawal discloses a method for simulating the execution of test vectors directed to specific electronic circuits; it is the examiner's position that a simulation of execution of a test vector to view the results of the simulation is a form of determination of the necessary memory require to execute the test vectors, and that Agrawal estimates the cost function by counting the remaining memory units unused by the circuit, which cannot be done without ascertaining the known or used memory units by the test vector. As a result of simulating the memory used by that test vector, Agrawal uses the unknown memory units to calculate the cost. Cost = a function of the total circuit memory minus the known memory). One could use the value of the total memory and count the known memory and subtract, or simply count the unknown units, either way it is dependent on the determined known memory units.

2. The appellant has argued on page 8 of brief; "*From the above excerpt, appellants believe it is dear that Agrawal does not disclose an action of "'determining a required memory needed to execute [a] plurality of test vectors", as the Examiner asserts.*" The examiner points to column 4 lines 33-38; "Such a simulator may be a computer program that accepts the circuit connectivity data and, for any given input stimulus vector, computes the output states of all gates in the circuit (for example, it may compute the output states for a digital circuit in terms of **0,** 1, or unknown--usually denoted by X)." By all gates in the circuit Agrawal means the flip-flops commonly known as memory gates. By denoting the value of 0, 1 or unknown, Agrawal is marking the memory used (or needed) for each stimulus vector; the unknown state are the ones the execution of the vector did not use.

3. The appellant has argued on page 10 of brief; "*Given that Agrawal does not disclose "determining a required memory needed to execute the plurality of test vectors"', it follows that Agrawal cannot disclose "using the required memory to estimate a cost to execute the test vectors." In particular, the "'cost function" disclosed by Agrawal is not "a cost to execute… [a plurality of] test vectors". Instead, Agrawal's "cost*

function" is an optimization function that is used to limit growth in a set of initialization vectors." The examiner points to Agrawal's budget constraints in column 5 lines 57-61; "But, one would rarely wish to select new vectors without regard to the computation costs (e.g. one would not wish to have a simulation that costs more than the budget would allow)." The examiner wishes to explain that Agrawal has "defined the cost of a fault as a weighted sum of its cost at the primary output and the various pseudo-outputs", (column 6 lines 62-65), and given these costs different weight values from 1 to 10. Agrawal has created an optimization cost function that is part of calculating the cost in dollars of testing the circuits since it has a relation with a budget. And further more, the language of independent claims 1, 8 and 13 do not differentiate between any type of cost function as a relation to money or optimization, simply claims 1, 8 and 13 state; "*using the required memory to estimate a cost to execute the test vectors.*"

4. The appellant has argued on page 11 of brief; "*Claims 2-5 and 7 are believed to be allowable, at least, because they depend from claim 1.*" And "*Claims 8-16 are believed to be allowable, at least, for reasons similar to why claim 1 is believed to be allowable.*" The argument is moot in view of the examiner's traverse of the above arguments brought forth to the rejection of claim 1.

5. The appellant has argued on page 11 of brief; "*Claims 3, 10 and I 5 are also believed to be allowable bemuse Agrawal fails to disclose that "determining a required memory comprises determining a required memory needed for* ***each of a plurality of boards of a tester*** *to execute the test vectors for the board." The Examiner asserts that this is disclosed in Agrawal's col. 6.50-68, in that Agrawal's "levels" of flip-flops are equivalent to different "boards of a tester"*" The examiner points to the language of claim 3; "a plurality of boards of a tester" and in view of the broad interpretation of the language: Circuit Board (e.g. *Electronics.* a sheet of insulating material used for the mounting and interconnection (often by a printed circuit) of components in electronic equipment). All testers are made of circuit boards circuit boards are the media where circuits are mounted and all devices are well known to have more than one board, thus one of ordinary skill in the art would have found the statement of claim 3 to mean for all the circuits applied to the tester, same as Agrawal's would be applied.

6. The appellant has argued on page 11 of brief; "*Claims 4, 11 and 16 are also believed to be allowable bemuse Agrawal fails to disclose that "determining a required memory comprises determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin,*" The appellant has agreed that Agrawal teaches testing the circuit as a whole, which means that every input point of the circuit was tested in order for the totality of the circuit to have been tested. The language of claim 4 does not indicate a test made "independently" to each pin, and would not been possible to test one input at a time unless they each had been an independent circuit.

7. The appellant has argued on page 12 of brief; "*Agrawal fails to disclose "determining a first memory requirement needed for* ***a first pin of a $ester*** *to execute the test vectors for a first test in the test file"; "determining a second memory requirement needed for [an]* ***additional pin*** *to execute the test vectors for the first test": and "if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement." Agrawal's comparisons of cost function values has nothing to do with comparing memory requirements.*" As covered in paragraph 6 above, the testing of Agrawal was for each input stimulus vector, thus every input (or pin) for the circuits is tested, and multiple vectors are simulated each input thus calculating the memory used by each vector.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/FRANK M LEIVA/

Examiner, Art Unit 3717

Conferees:

/Melba Bumgarner/

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